Module 6: Oscillators and Current Mirrors

Module 6 Overview:

This module introduces two critical concepts in analog circuit design: oscillators, which generate repetitive waveforms, and current mirrors, fundamental building blocks for precise current biasing. We will begin by exploring the basic principles required for sustained oscillations, delving into the essential Barkhausen Criterion. We will then analyze various types of sinusoidal oscillators, including RC and LC configurations, deriving their operating frequencies and oscillation conditions. The module will also briefly touch upon non-sinusoidal oscillators. Finally, we will shift focus to current mirrors, examining their basic topology, crucial variants like Wilson and Widlar mirrors, and their key performance characteristics such as V-I characteristics, output resistance, and maximum usable load.

6.1 Review of Basic Oscillator Concepts: Conditions for Sustained Oscillations

Introduction:

An oscillator is an electronic circuit that produces a repetitive, oscillating electronic signal, often a sine wave or a square wave, without the need for an external input signal. Unlike amplifiers, which magnify an input, oscillators generate their own output from DC power supplies. They are essential in numerous applications, including clock generators in digital systems, radio frequency (RF) communications, signal generators, and timing circuits.

Basic Concept:

At its core, an oscillator consists of two main parts:

1. **An Amplifier:** To provide gain and compensate for energy losses in the circuit.
2. **A Feedback Network:** To return a portion of the amplifier's output back to its input.

How Oscillation Starts and Sustains:

1. **Noise:** When power is first applied to an oscillator circuit, there's always some random electrical noise present. This noise contains components at various frequencies.
2. **Amplification:** The amplifier magnifies these noise components.
3. **Frequency Selection (Feedback Network):** The feedback network is designed to be frequency-selective. It allows only a specific frequency (or a narrow band of frequencies) to pass through with the correct phase.
4. **Positive Feedback:** The crucial element for oscillation is positive feedback. This means the signal fed back to the input must be in phase with the original input signal at the desired oscillation frequency. This reinforcement causes the signal at that specific frequency to grow.
5. **Sustained Oscillation:** If the loop gain (product of amplifier gain and feedback network gain) is precisely unity (1) at the oscillation frequency, the signal will continue

to oscillate indefinitely at a constant amplitude. If the loop gain is greater than unity, the oscillation amplitude will grow until limited by the amplifier's non-linearity (clipping). If the loop gain is less than unity, the oscillations will die out.

Conditions for Sustained Oscillations:

For an oscillator to produce sustained, stable oscillations, two primary conditions must be met:

1. **Phase Condition (or Phase Shift Condition):** The total phase shift around the closed loop (amplifier phase shift + feedback network phase shift) must be an integer multiple of 360 degrees (or 0 degrees, which is $0^\\circ, 360^\\circ, 720^\\circ$, etc.).
    - This ensures that the fed-back signal reinforces the original input signal.
    - For a non-inverting amplifier, the feedback network must provide 0 degrees phase shift.
    - For an inverting amplifier (e.g., common emitter BJT or common source FET without emitter/source degeneration, or an op-amp in inverting configuration), the feedback network must provide 180 degrees phase shift so that the total loop phase shift is $180^\\circ + 180^\\circ = 360^\\circ$.
2. **Magnitude Condition (or Gain Condition):** The magnitude of the loop gain (|Abeta|, where A is the amplifier gain and beta (beta) is the feedback network gain) must be equal to or slightly greater than unity (1) at the oscillation frequency.
    - |Abeta|ge1
    - If |Abeta|1, the amplitude grows until non-linearities (like saturation or cutoff of the transistor) limit it.
    - If $|A\\beta| \< 1$, the oscillations die out.
    - In practical circuits, the loop gain is often designed to be slightly greater than 1 initially to ensure oscillations start reliably, and then non-linear mechanisms limit the amplitude to a stable level.

These two conditions are formally summarized by the Barkhausen Criterion.

6.2 Barkhausen Criterion: The Fundamental Principle of Oscillation

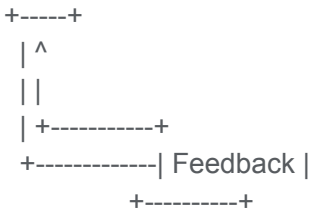
Introduction:

The Barkhausen Criterion, named after Heinrich Georg Barkhausen, provides the mathematical conditions necessary for an electronic circuit to sustain oscillations. It formalizes the phase and magnitude conditions discussed previously for positive feedback systems.

Mathematical Formulation:

Consider a feedback system as shown:

```
          +-----+
Input  -----> | Amp | -----> Output
```



The voltage fed back to the input (V_f) is given by $V_f=\beta V_{out}$, where β is the transfer function (gain) of the feedback network.

The output voltage (V_{out}) is given by $V_{out}=AV_{in}$, where A is the voltage gain of the amplifier.

For positive feedback, V_{in} is effectively the fed-back signal itself when the external input is removed. So, $V_{in}=V_f$.

Substituting these, we get:

$V_{out}=A(\beta V_{out})$

Dividing by V_{out} (assuming $V_{out} \neq 0$ for oscillations):

$A\beta=1$

This equation, $A\beta=1$, is the mathematical representation of the Barkhausen Criterion. It is a complex number equation, implying both magnitude and phase.

Conditions derived from Barkhausen Criterion:

1. Phase Condition: The phase of the loop gain $A\beta$ must be 0 degrees or an integer multiple of 360 degrees.
   $\angle(A\beta)=2n\pi \text{ or } n\times 360^\circ$ (where $n=0,1,2,\ldots$)
   This ensures that the fed-back signal is in phase with the original input signal, leading to constructive interference.
2. Magnitude Condition: The magnitude of the loop gain $A\beta$ must be equal to or greater than unity (1).
   $|A\beta| \geq 1$
   This ensures that the amplitude of the oscillations can grow or be sustained. If it's exactly 1, the oscillations are sustained at a constant amplitude. If it's slightly greater than 1, the oscillations build up, and non-linearities in the amplifier limit the amplitude to a stable value where the effective $|A\beta|$ becomes 1.

Application:

To design an oscillator, one typically starts by designing a feedback network that provides the required phase shift (e.g., 180° for an inverting amplifier) at the desired oscillation frequency. Then, an amplifier is chosen or designed to provide sufficient gain at that frequency to satisfy the magnitude condition. The total phase shift around the loop will then be 360° (or 0°).

6.3 RC Oscillators

Introduction:

RC oscillators use resistors and capacitors in their feedback networks to achieve the necessary phase shift and frequency selectivity. They are generally suitable for lower frequencies (up to a few MHz) and are known for their good frequency stability at these ranges. The phase shift of an RC network depends on frequency, allowing for frequency selection.

6.3.1 Phase Shift Oscillator

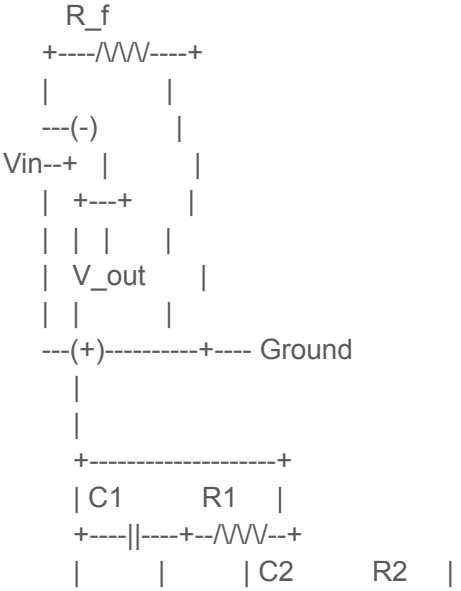
Circuit Analysis:

A phase shift oscillator typically consists of an inverting amplifier (e.g., a common-emitter BJT stage, a common-source FET stage, or an op-amp in an inverting configuration) and a three-section (or sometimes four-section) RC ladder network. Each RC section in the ladder network provides a phase shift, and for oscillation, the total phase shift from the RC network must be 180 degrees. Since the amplifier itself provides 180 degrees phase shift (being inverting), the total loop phase shift becomes $180^\\circ + 180^\\circ = 360^\\circ$ (or $0^\\circ$).

RC Ladder Network:

Each RC section provides a maximum phase shift of 90 degrees. However, cascaded identical sections don't simply add their individual maximum shifts. For three identical cascaded RC sections, the total phase shift approaches 180 degrees at a specific frequency, but never quite reaches it without attenuation. A common configuration uses three identical RC sections, where each section contributes 60 degrees of phase shift at the oscillation frequency.

Circuit Diagram (Conceptual for Op-Amp):



```
|         +----||----+--/\/\/--+
|         |          |         | C3          R3     |
|         |          |         +----||----+--/\/\/--+---- Ground
|         |          |         |          |
+----------+----------+----------+----------+
Feedback from Output to Vin (negative input of op-amp)
```

Frequency Determination:

For a three-section RC phase shift network with identical R and C components ($R_1=R_2=R_3=R$, $C_1=C_2=C_3=C$), the oscillation frequency (f_0) is given by:

$$f_0=\frac{1}{2\pi RC\sqrt{6}}$$

Condition for Oscillation (Magnitude Condition):

At this frequency, the feedback network introduces an attenuation of 1/29. This means the amplifier must have a voltage gain ($|A_v|$) of at least 29 to compensate for this attenuation and satisfy the Barkhausen criterion.

$$|Av|\geq 29$$

Derivation (Simplified):

The derivation involves analyzing the transfer function of the RC ladder network and finding the frequency at which the phase shift is 180°. At this frequency, the magnitude of the transfer function is determined.

For the three-stage RC ladder network, the feedback factor beta is:

$$\beta=\frac{1}{1-5(\omega RC)^2+j(6\omega RC-(\omega RC)^3)}$$

For the phase shift to be 180°, the imaginary part must be zero:

$$6\frac{1}{\omega RC}-\left(\frac{1}{\omega RC}\right)^3=0$$

$$\frac{1}{\omega RC}\left(6-\left(\frac{1}{\omega RC}\right)^2\right)=0$$

Since $\frac{1}{\omega RC}\neq 0$, we have $6-\left(\frac{1}{\omega RC}\right)^2=0$.

$$\left(\frac{1}{\omega RC}\right)^2=6$$

$$\frac{1}{\omega RC}=\sqrt{6}$$

$$\omega=\frac{1}{RC\sqrt{6}}$$

Since $\omega=2\pi f_0$:

$$f_0=\frac{1}{2\pi RC\sqrt{6}}$$

At this frequency, substituting frac1omegaRC=sqrt6 back into the magnitude part of beta:

beta=frac11−5(6)=frac11−30=−frac129

The negative sign indicates the $180^\\circ$ phase shift. Thus, for oscillation, the amplifier gain |A_v| must be 29.

Numerical Example:

Design a phase shift oscillator using an op-amp for f_0=1textkHz. Let C=10textnF.

R=frac12pif_0Csqrt6=frac12pitimes1000textHztimes10times10−9textFtimessqrt6

R=frac12pitimes10−5timessqrt6textOmega=frac16.283times10−5times2.449textOmega=frac11.539times10−4textOmegaapprox6497textOmega.

Use standard resistor value R=6.8textkOmega.

The op-amp should be configured for an inverting gain of at least 29. If using feedback resistors R_f and R_in (for the op-amp input), A_v=R_f/R_in. So, R_f/R_inge29. If R_in=1textkOmega, then R_fge29textkOmega.

6.3.2 Wien Bridge Oscillator

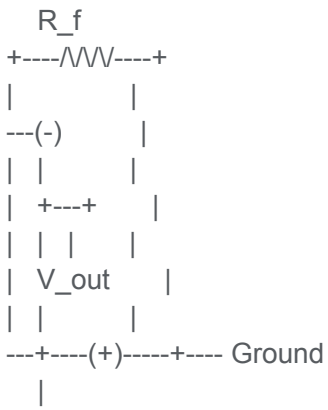
Circuit Analysis:

The Wien Bridge oscillator is one of the most popular and historically significant RC oscillators, particularly for audio frequencies (Hz to hundreds of kHz). It uses a bridge circuit in its feedback network and is typically implemented with a non-inverting amplifier (e.g., an op-amp in a non-inverting configuration).

Wien Bridge Network:

The feedback network consists of a series RC circuit and a parallel RC circuit, forming two arms of a bridge. This network provides a 0-degree phase shift at a specific frequency and acts as a band-pass filter.

Circuit Diagram (Conceptual for Op-Amp):



```
|
| R4
+--/\/\/--+
|          |
+----------+
| C_series
+----||-----+
|          |
| R_parallel
+----/\/\/--+---- Ground
|          |
| C_parallel
+----||-----+---- Ground
Feedback from Output to (+) input of op-amp
```

Frequency Determination:

For the simplest case where R_series=R_parallel=R and C_series=C_parallel=C, the oscillation frequency (f_0) is given by:

f0=2πRC1
Condition for Oscillation (Magnitude Condition):

At this frequency, the Wien bridge network has an attenuation of 1/3. Therefore, the non-inverting amplifier must have a voltage gain (∣A_v∣) of at least 3 to satisfy the Barkhausen criterion.

∣Av∣≥3
Derivation (Simplified):

The transfer function of the Wien bridge network (V_feedback/V_out) for identical R and C is:

β=1+3jωRC−(ωRC)2jωRC
For the phase shift to be $0^\\circ$, the imaginary part must be zero (assuming a real denominator for zero phase):

1−(omegaRC)2=0

(omegaRC)2=1

omegaRC=1

omega=frac1RC

Since omega=2pif_0:

f_0=frac12piRC

At this frequency, substitute omegaRC=1 back into beta:

β=1+3j(1)−(1)2j(1)=1+3j−1j=3jj=31
Thus, for oscillation, the amplifier gain $|A_v|$ must be 3. In op-amp implementations, the non-inverting gain is 1+R_f/R_i. So, 1+R_f/R_i=3, which means R_f/R_i=2.

Numerical Example:

Design a Wien bridge oscillator for f_0=10textkHz. Let C=1textnF.

R=frac12pif_0C=frac12pitimes10000textHztimes1times10−9textF

R=frac12pitimes10−5textOmega=frac16.283times10−5textOmegaapprox15915textOmega.

Use standard resistor value R=16textkOmega.

The non-inverting op-amp gain should be 3. If the feedback resistors are R_f and R_i for the non-inverting amplifier, then 1+R_f/R_i=3impliesR_f/R_i=2. For instance, R_i=10textkOmega and R_f=20textkOmega.

6.4 LC Oscillators

Introduction:

LC oscillators use inductors (L) and capacitors (C) in their feedback networks. They are typically used for higher frequencies (MHz to GHz) because the impedance of capacitors becomes very low and inductors very high at high frequencies, making RC components impractical. LC tank circuits are resonant circuits that naturally oscillate at a specific frequency, and this characteristic is exploited in LC oscillators.

Basic LC Tank Circuit:

An LC tank circuit (parallel LC) stores energy and oscillates at its resonant frequency:

fr=2πLC 1
In LC oscillators, the amplifier provides the energy to compensate for losses in the tank circuit, maintaining sustained oscillation.

6.4.1 Hartley Oscillator

Circuit Analysis:

The Hartley oscillator uses a tapped inductor (or two inductors in series with a common connection) and a single capacitor in its tank circuit. The feedback is obtained from the inductor tap. It is characterized by having the resonant circuit in the collector/drain/plate circuit and deriving feedback from the inductive divider.

Configuration:

The feedback network consists of L_1, L_2 (in series), and a parallel capacitor C. The junction of L_1 and L_2 is often connected to the emitter/source of the transistor, or to ground through a DC block. The feedback signal is derived from the voltage across L_1 relative to the voltage across L_2.

Circuit Diagram (Conceptual for BJT):

```
    VCC
     |
     Rb1
     |
     |     L_choke
     +-----/\/\/----+
     |              |
     Rc             |
    ---/\/\/---+    |
    |          |    C
    |          +----||----+
    |          |    |    |
    |          |    |    Rb2
    Q          +----+    |
    | Base     | Emitter  |
    +----------+----------+---- Ground
    |         L1         L2
    +----UUUU----+----UUUU----+
    |          |
    C_c        | (connection point for feedback)
    |          |
    +----------+---- Ground
    Input from feedback network to Base
```

(Self-correction: A clearer diagram of the tank circuit connected to the amplifier is needed.)

In a typical BJT Hartley oscillator:

- The collector is connected to the top of L_1 (via a coupling capacitor or choke).
- The emitter is connected to the tap between L_1 and L_2.
- The base provides the input from the feedback.
  The output is taken from the collector or across the tank.

Frequency Determination:

The oscillation frequency (f_0) for a Hartley oscillator is determined by the total inductance of the series inductors (L_eq=L_1+L_2+2M, where M is mutual inductance, often neglected or designed to be zero) and the capacitance C.

$$f_0 = \frac{1}{2\pi \sqrt{(L_1 + L_2)C}}$$If there is mutual inductance M between L_1 and L_2:

f0=2π(L1+L2+2M)C  1
Condition for Oscillation (Magnitude Condition):

For sustained oscillations, the amplifier's current gain (h_fe or beta for BJT) or voltage gain must compensate for the losses. The minimum gain requirement depends on the specific biasing and transistor parameters.

A common approximation for minimum current gain (h_fe) is:

hfe≥L2L1
This indicates that a larger L_1 relative to L_2 requires a larger gain from the amplifier.

Numerical Example:

Design a Hartley oscillator with L_1=1textmH, L_2=100textμH, and C=100textpF. Assume no mutual inductance.

1. Calculate Oscillation Frequency:
   L_eq=L_1+L_2=1textmH+0.1textmH=1.1textmH
   f_0=frac12pisqrt(1.1times10−3textH)(100times10−12textF)
   f_0=frac12pisqrt1.1times10−13=frac12pitimes3.317times10−7approx480textkHz
2. Minimum Gain Requirement:
   h_fegefracL_1L_2=frac1textmH0.1textmH=10
   The transistor used in the amplifier should have a beta (or h_fe) of at least 10 at the operating frequency.

6.4.2 Colpitts Oscillator

Circuit Analysis:

The Colpitts oscillator uses a tapped capacitor (or two capacitors in series) and a single inductor in its tank circuit. The feedback is obtained from the capacitor tap. It is essentially the dual of the Hartley oscillator.

Configuration:

The feedback network consists of C_1, C_2 (in series), and a parallel inductor L. The junction of C_1 and C_2 is typically connected to the emitter/source or ground, and feedback is provided from the capacitive divider.

Circuit Diagram (Conceptual for BJT):

```
VCC
 |
 Rb1
 |
```

```
|      L
+-----UUUU-----+
|              |
Rc             C1
---/\/\/\---+--||----+
|           |        |
|           |        |
Q           +---------+----- Ground
| Base      | Emitter |
+-----------+---------+
|           C2
C_c         ||
|           |
+-----------+----- Ground
Input from feedback network to Base
```

(Self-correction: A clearer diagram of the tank circuit connected to the amplifier is needed.)

In a typical BJT Colpitts oscillator:

- The collector is connected to the top of L (via a coupling capacitor or choke).
- The emitter is connected to the junction of C_1 and C_2.
- The base provides the input from the feedback.
  The output is taken from the collector or across the tank.

Frequency Determination:

The oscillation frequency (f_0) for a Colpitts oscillator is determined by the total equivalent capacitance of the series capacitors (C_eq=fracC_1C_2C_1+C_2) and the inductance L.

f0=2πLCeq 1=2πLC1+C2C1C2 1
Condition for Oscillation (Magnitude Condition):

Similar to the Hartley oscillator, the amplifier gain must be sufficient to compensate for losses.

A common approximation for minimum current gain (h_fe) is:

hfe≥C1C2
This means a larger C_2 relative to C_1 requires a larger gain from the amplifier.

Numerical Example:

Design a Colpitts oscillator with L=100textμH, C_1=100textpF, and C_2=1textnF.

1. Calculate Equivalent Capacitance:
   $C_{eq}=\frac{C_1C_2}{C_1+C_2}=\frac{(100\times10^{-12}\text{F})(1\times10^{-9}\text{F})}{100\times10^{-12}\text{F}+1\times10^{-9}\text{F}}$
   $C_{eq}=\frac{10^{-19}}{1.1\times10^{-9}}=\frac{10^{-10}}{1.1}\text{F}\approx90.9\text{pF}$
2. Calculate Oscillation Frequency:
   $f_0=\frac{1}{2\pi\sqrt{(100\times10^{-6}\text{H})(90.9\times10^{-12}\text{F})}}$
   $f_0=\frac{1}{2\pi\sqrt{9.09\times10^{-15}}}=\frac{1}{2\pi\times9.53\times10^{-8}}\approx1.67\text{MHz}$
3. Minimum Gain Requirement:
   $h_{fe}\geq\frac{C_2}{C_1}=\frac{1\text{nF}}{100\text{pF}}=\frac{1000\text{pF}}{100\text{pF}}=10$
   The transistor should have a beta of at least 10.

6.4.3 Clapp Oscillator

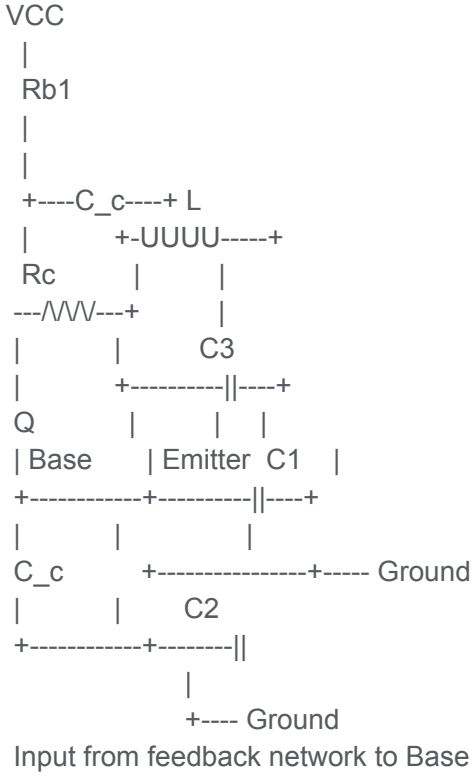
Circuit Analysis:

The Clapp oscillator is a variation of the Colpitts oscillator designed for improved frequency stability. It adds an additional capacitor (C_3) in series with the inductor (L) in the tank circuit. This capacitor effectively isolates the tank circuit's resonant frequency from the transistor's parasitic capacitances, leading to better frequency stability.

Configuration:

The Clapp oscillator uses C_1 and C_2 in series (like Colpitts) but places a third capacitor C_3 in series with the inductor L. The overall equivalent capacitance that determines the frequency is then a combination of C_1, C_2, and C_3.

Circuit Diagram (Conceptual for BJT):



(Self-correction: A clearer diagram of the tank circuit connected to the amplifier is needed.)

Frequency Determination:

The oscillation frequency (f_0) for a Clapp oscillator is determined by the inductor L and the equivalent capacitance C_eq′, where C_eq′ is the series combination of C_1, C_2, and C_3.

The equivalent capacitance of the three series capacitors is:

$$\frac{1}{C_{eq}'} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$Therefore, the oscillation frequency is:

f0=2πLCeq′1

f0=2πL(C11+C21+C311)1
Condition for Oscillation (Magnitude Condition):

The gain condition is similar to the Colpitts oscillator, given by:

hfe≥C1C2
However, the inclusion of C_3 makes the effective C_eq smaller, which means the frequency is primarily controlled by C_3 (if C_3 is much smaller than C_1 and C_2). This is what provides the better stability.

Numerical Example:

Design a Clapp oscillator with L=100textμH, C_1=1textnF, C_2=1textnF, and C_3=100textpF.

1. Calculate Equivalent Capacitance:
   frac1C_eq′=frac11textnF+frac11textnF+frac1100textpF
   frac1C_eq′=frac110−9+frac110−9+frac110−10
   frac1C_eq′=109+109+1010=2times109+10times109=12times109textF−1
   C_eq′=frac112times109textFapprox83.33textpF
2. Calculate Oscillation Frequency:
   f_0=frac12pisqrt(100times10−6textH)(83.33times10−12textF)
   f_0=frac12pisqrt8.333times10−15=frac12pitimes9.128times10−8approx1.74textMHz
3. Minimum Gain Requirement:
   h_fegefracC_2C_1=frac1textnF1textnF=1
   This indicates a very low gain requirement due to C_1 and C_2 being relatively large, making it easier to achieve oscillation.

6.5 Non-Sinusoidal Oscillators (Relaxation Oscillators): Basic Principles (e.g., Astable Multivibrator using 555 timer - brief)

Introduction:

While sinusoidal oscillators produce smooth, continuous sine waves, non-sinusoidal oscillators (also known as relaxation oscillators) generate square waves, triangular waves, sawtooth waves, or pulse waveforms. These oscillators rely on the charging and discharging of a capacitor (or inductor) through a resistor, coupled with a switching device that changes state when a certain voltage threshold is reached.

Basic Principles of Relaxation Oscillators:

1. **Energy Storage Element:** A capacitor is charged through a resistor (or current source).
2. **Threshold Detector:** A circuit monitors the voltage across the capacitor.
3. **Switching Device:** When the capacitor voltage reaches an upper threshold, a switching device (e.g., transistor, Schmitt trigger, comparator) activates.
4. **Discharge Path:** The switching device then provides a path for the capacitor to discharge, often through a different resistor.
5. **Lower Threshold:** When the capacitor voltage drops to a lower threshold, the switching device deactivates, and the cycle repeats.

The charging and discharging rates, determined by RC time constants, dictate the frequency and duty cycle of the output waveform.

Astable Multivibrator using 555 Timer:

The 555 timer IC is a versatile and widely used integrated circuit for timing and oscillation applications, particularly for generating square wave (or pulse) outputs. When configured as an astable multivibrator, it operates as a free-running oscillator, continuously producing a rectangular waveform.

How it Works (Briefly):

The 555 timer has two internal comparators, a flip-flop, and a discharge transistor.

- **Charging:** A capacitor (C) charges through two external resistors (R_A and R_B) towards the supply voltage.
- **Upper Threshold (Triggering):** When the capacitor voltage reaches 2/3 of the supply voltage (VCC), the "Threshold" comparator triggers the internal flip-flop. This causes the output to go low and activates the "Discharge" transistor.
- **Discharging:** The activated discharge transistor provides a path for the capacitor to discharge through R_B towards ground.
- **Lower Threshold (Triggering):** When the capacitor voltage drops to 1/3 of the supply voltage, the "Trigger" comparator triggers the flip-flop again. This causes the output to go high and deactivates the discharge transistor.
- **Cycle Repeats:** The capacitor begins charging again, and the cycle repeats, creating a continuous square wave output.

Frequency and Duty Cycle:

The frequency (f) and duty cycle of the 555 astable multivibrator are determined by the values of R_A, R_B, and C.

- Frequency:
  f=(RA+2RB)C1.44
- Duty Cycle (D): The percentage of time the output is high.
  D=RA+2RBRA+RB×100%
  Note that the duty cycle is always greater than 50% for this standard configuration because R_A is present during both charging and discharging. To achieve a 50% duty cycle, a diode can be placed in parallel with R_B to bypass R_B during charging.

Numerical Example:

Design a 555 astable multivibrator for approximately 10textkHz with R_A=1textkOmega and R_B=10textkOmega.

1. Calculate Capacitor Value:
   C=frac1.44(R_A+2R_B)f=frac1.44(1000+2times10000)textOmegatimes10000textHz
   C=frac1.44(1000+20000)times10000textF=frac1.4421000times10000textF=frac1.442
   .1times108textFapprox6.86times10−9textF=6.86textnF.
   Use standard capacitor C=6.8textnF.
2. Calculate Duty Cycle:
   D=frac1textkOmega+10textkOmega1textkOmega+2times10textkOmegatimes100

6.6 Current Mirror

Introduction:

A current mirror is a fundamental circuit block in analog integrated circuits (ICs) that is used to "copy" or "mirror" a reference current from one part of a circuit to another. It works on the principle that identical transistors operating at the same temperature and having the same base-emitter (or gate-source) voltage will have approximately the same collector (or drain) current. Current mirrors are essential for biasing, active loads, and differential amplifier stages because they provide stable and precise current sources or sinks.

6.6.1 Basic Topology: Operation and Importance

Basic BJT Current Mirror:

The most common basic current mirror uses two matched BJTs.

Circuit Diagram (Conceptual):

```
VCC
 |
```

```
R_ref
|
+----/\/\/----+
|             |
Q1 Base        Q2 Base
+-----+---------+
|     |         |
C1    C2        Collector of Q2 (Output)
|     |         |
E1    E2        Emitter of Q2
|     |         |
+-----+---------+---- Ground
|
+---- Current Ref (I_ref)
|
+---- Diode connected Q1
```

(Self-correction: A proper circuit diagram for the basic BJT current mirror is required.)

Operation:

1. **Reference Transistor (Q1):** One transistor (Q1) is "diode-connected," meaning its collector is shorted to its base. This configuration forces Q1 to operate in the active region (or saturation for FETs). A reference current (I_ref) is established through Q1.
    - The current I_ref can be set by a resistor from VCC or by another current source.
    - The base-emitter voltage (V_BE1) of Q1 is determined by I_ref. Because Q_1 is diode-connected, its collector current is approximately equal to its emitter current.
    - I_ref=I_C1+I_B1approxI_C1(1+1/beta). If beta is large, I_refapproxI_C1.
2. **Mirror Transistor (Q2):** The base of Q2 is connected directly to the base of Q1. Since the bases are connected, V_BE2=V_BE1.
    - If Q1 and Q2 are identical (matched) and at the same temperature, and V_BE1=V_BE2, then their collector currents will be approximately equal.
    - I_C2=I_C1 (assuming identical transistors and ideal conditions).
    - The current I_C2 becomes the "mirrored" output current (I_out).

Importance:

- **Current Biasing:** Provides stable and precise DC bias currents for various stages in an IC, such as amplifiers and differential pairs.
- **Active Loads:** Replaces resistors as loads in amplifier stages, leading to higher voltage gain and better efficiency.
- **Matching:** By integrating on a chip, transistors can be fabricated very close to each other, ensuring excellent matching of characteristics.
- **Current Sources/Sinks:** Can act as constant current sources (sourcing current into a load) or constant current sinks (sinking current from a load).

Key Equation (Ideal BJT Mirror):

If Q_1 and Q_2 are matched and beta is large:

$$I_{out} = I_{ref}$$More accurately, accounting for base currents:

Iref=IC1+2IB=IC1+2βIC1=IC1(1+β2)
Iout=IC2=IC1=1+β2Iref
This shows that I_out is slightly less than I_ref due to the base currents.

Basic MOSFET Current Mirror:

Similar principles apply to MOSFETs.

Circuit Diagram (Conceptual):

```
VDD
 |
 R_ref
 |
 +----/\/\/\----+
 |              |
 D1             D2 (Output)
 |              |
 G1             G2
 +-----+---------+
 |     |        |
 S1    S2
 |     |        |
 +-----+---------+---- Ground
 |
 +---- Current Ref (I_ref)
 |
 +---- Gate connected to Drain for M1
```

(Self-correction: A proper circuit diagram for the basic MOSFET current mirror is required.)

Operation:

1. **Reference Transistor (M1):** M1 is diode-connected (gate shorted to drain). This forces V_DS1=V_GS1. M1 operates in saturation if V_GS1V_th. I_ref flows through M1, setting its V_GS1.
2. **Mirror Transistor (M2):** The gate of M2 is connected to the gate of M1. So V_GS2=V_GS1.
3. If M1 and M2 are identical and in saturation, then I_D2=I_D1. Thus I_out=I_ref.
    - MOSFET current mirrors are generally preferred in ICs because their input impedance is ideally infinite (no gate current), meaning no base current loss like in BJTs.

Key Equation (Ideal MOSFET Mirror):

If M1 and M2 are matched:

$$I_{out} = I_{ref}$$If their (W/L) ratios are different:

Iout=Iref×(W/L)1(W/L)2
This allows for scaling of the mirrored current.

6.6.2 Variants of Current Mirrors: Wilson, Widlar, etc.

While the basic current mirror is simple, it suffers from limitations, primarily due to the Early effect (finite output resistance) and base current mismatch in BJTs. Various improved topologies have been developed.

A. Wilson Current Mirror (BJT or MOSFET):

The Wilson current mirror (also known as a three-transistor mirror) improves the output resistance and reduces the error due to base currents compared to the basic mirror.

Advantages:

- **Higher Output Resistance:** Significantly increased output resistance, making it behave more like an ideal current source. This is due to negative feedback inherent in the structure.
- **Reduced Base Current Error:** For BJTs, it helps to mitigate the effect of finite beta on the output current accuracy.

Disadvantage:

- **Higher Minimum Output Voltage (Voltage Headroom):** Requires a higher minimum voltage across the output (collector-emitter or drain-source) to maintain proper operation, which can limit the output voltage swing.

Basic Idea: It adds an extra transistor to buffer the base currents, ensuring that the reference current primarily flows through the diode-connected transistor, and another transistor to provide negative feedback, increasing output resistance.

B. Widlar Current Mirror (BJT only):

The Widlar current mirror is specifically designed to create small output currents (I_out) from a larger reference current (I_ref) without requiring large resistors. This is particularly useful for low-power applications.

Advantages:

- **Generates Small Currents:** Can produce output currents that are significantly smaller than the reference current by adding a resistor in the emitter of the output transistor.

- **Lower Resistance Values:** Avoids the need for very large (and space-consuming) resistors to generate small currents.

Operation:

A resistor (R_E) is added in the emitter of the output transistor (Q2). This creates a voltage drop across R_E, reducing V_BE2 relative to V_BE1. Since I_C is exponentially related to V_BE, even a small difference in V_BE can lead to a large difference in I_C.

Key Equations (Widlar Mirror):

Assuming matched transistors and neglecting base currents for simplification:

V_BE1−V_BE2=I_E2R_EapproxI_C2R_E=I_outR_E

Also, V_BE1−V_BE2=V_Tln(fracI_C1I_C2)=V_Tln(fracI_refI_out)

Equating these:

IoutRE=VTln(IoutIref)
This equation must be solved iteratively or graphically to find I_out for given I_ref and R_E.

This allows I_out to be much smaller than I_ref.

Disadvantage:

- **Sensitivity to Temperature:** The V_T term makes the output current more sensitive to temperature variations.
- **Slightly Lower Output Resistance:** The output resistance is typically dominated by r_o of the output transistor and the feedback effect of R_E.

6.6.3 V-I Characteristics: Output Resistance and Minimum Sustainable Voltage (V_ON)

V-I Characteristics (Output Current vs. Output Voltage):

The ideal current mirror should provide a constant output current (I_out) regardless of the voltage across its output terminals (V_CE2 for BJT, V_DS2 for MOSFET). However, in practical current mirrors, the output current shows some dependence on the output voltage.

- **For BJT Current Mirror:** The output characteristic (I_C2 vs. V_CE2) resembles the output characteristics of a single BJT in the active region. As V_CE2 increases, I_C2 slightly increases due to the Early effect.
- **For MOSFET Current Mirror:** The output characteristic (I_D2 vs. V_DS2) resembles the output characteristics of a single MOSFET in saturation. As V_DS2 increases, I_D2 slightly increases due to channel-length modulation.

Output Resistance (R_out):

Output resistance is a measure of how well the current mirror acts as a constant current source. An ideal current source has infinite output resistance.

- Basic BJT Current Mirror: The output resistance is primarily the output resistance of the transistor Q2, which is r_o2 (due to Early effect).
  Rout=ro2=IoutVA
- Basic MOSFET Current Mirror: The output resistance is primarily the output resistance of the transistor M2, which is r_o2 (due to channel-length modulation).
  Rout=ro2=λIout1
  Where lambda is the channel-length modulation parameter.
- Wilson Current Mirror: Significantly higher output resistance, typically orders of magnitude greater than the basic mirror.
  For BJT Wilson mirror: R_outapproxbetar_o2. (More precisely, includes r_o3 and other terms)
  For MOSFET Wilson mirror: R_outapproxg_m3r_o3r_o2. (Product of transconductance and output resistances)
- Widlar Current Mirror: The output resistance is also enhanced by the emitter resistor.
  Rout=ro2(1+gm2RE)
  This shows the benefit of R_E in increasing output resistance.

Minimum Sustainable Voltage (V_ON or Compliance Voltage):

This is the minimum voltage drop required across the current mirror's output terminals for it to operate correctly and supply the intended current. Below this voltage, the output transistor comes out of saturation (for MOSFETs) or active region (for BJTs), and the mirrored current deviates significantly from the desired value.

- Basic BJT Current Mirror: For Q2 to be in the active region, V_C2 must be greater than V_B2−0.4textV (approximately). Since V_B2=V_BE1, V_ONapproxV_BE1(on). So, V_ONapproxV_BE(on) (typically 0.7textV).
- Basic MOSFET Current Mirror: For M2 to be in saturation, V_DS2geV_GS2−V_th. Since V_GS2=V_GS1, and V_DS1=V_GS1, the minimum output voltage is V_DS2(min)=V_GS1.
  VON=VGS(on)
- Wilson Current Mirror: Requires higher V_ON due to the series connection of transistors.
  For BJT Wilson mirror: V_ONapproxV_BE1+V_CE(sat)_Q3approxV_BE+0.2textV (approx 0.9textV).
  For MOSFET Wilson mirror: V_ONapprox2V_GS(on).
- **Widlar Current Mirror:** The V_ON is approximately V_BE(on) plus the voltage drop across R_E. V_ONapproxV_CE(sat)_Q2+I_outR_E. Or simply V_CE(sat)_Q2 as R_E does not add to the minimum V_CE. The minimum output voltage to maintain active region for Q2 is typically V_CE(sat), which is around 0.2textV.

A lower V_ON is desirable because it allows the current mirror to operate over a wider range of output voltages, providing more headroom for the load.

6.6.4 Maximum Usable Load

Introduction:

The "maximum usable load" for a current mirror refers to the maximum resistance or voltage drop that the current mirror can drive while still maintaining its intended function as a constant current source. It's related to the compliance voltage (V_ON) and the available power supply.

Concept:

A current mirror needs a certain minimum voltage across its output terminals (V_ON) to remain in its active (BJT) or saturation (MOSFET) region and deliver the constant current. If the voltage drop across the load (I_outtimesR_load) plus the minimum voltage required by the mirror (V_ON) exceeds the available supply voltage (V_supply), the mirror will "fall out of compliance," and its output current will no longer be constant.

Equation for Maximum Usable Load (Resistive Load):

For a current mirror driving a resistive load R_load:

The voltage across the load is V_load=I_outtimesR_load.

The voltage across the current mirror's output is V_output_mirror.

For proper operation:

V_supplygeV_output_mirror+V_load

V_supplygeV_ON+I_outR_load

Therefore, the maximum usable load resistance (R_load(max)) is:

Rload(max)=IoutVsupply−VON
If the load is a more complex circuit, the concept extends to ensuring that the voltage at the output terminal of the current mirror does not drop below V_ON.

Numerical Example:

Consider a basic BJT current mirror designed to supply I_out=1textmA from a V_CC=5textV supply. Assume V_ON=0.7textV (for the basic mirror).

Calculate the maximum usable load resistance:

R_load(max)=fracV_CC−V_ONI_out=frac5textV−0.7textV1textmA

R_load(max)=frac4.3textV1times10−3textA=4300textOmega=4.3textkOmega

This means if you connect a load resistor greater than 4.3textkOmega to this current mirror, the voltage across the mirror's output will drop below 0.7textV, and it will no longer function

as a constant 1textmA source. The current will start to decrease as the load resistance increases beyond this point.

The concept of maximum usable load (or compliance voltage) is crucial for designing circuits where current mirrors are used to bias other stages, ensuring that these stages receive the correct current while allowing sufficient voltage swing.
